IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: John X. Zhong, et al.

Assignee: Synopsys, Inc.

Title: DESIGN VERIFICATION BY SYMBOLIC SIMULATION USING A NATIVE HARDWARE DESCRIPTION LANGUAGE

Serial No.: 10/620,628 File Date: 07/15/2003

Examiner: Stacy Whitmore Art Unit: 2825

Docket No.: SYN-0551CON1 (formerly 4162P001C)

Date: September 14, 2005

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

AMENDMENT IN RESPONSE TO THE FIRST OFFICE ACTION

Summary:

In the present application, Claims 1, 2, 4, 6-12, 14, and 16-20 are pending. In the present paper, Claims 1, 2, 4, 7, 11, 14, and 15 are amended, and Claims 3 and 13 are cancelled. Claims 1-4, 6-14, and 16-20 stand rejected under the judicially created doctrine of obviousness-type double patenting, as being unpatentable over Claims 1-18 of U.S. Patent No. 6,634,012, issued October 14, 2003 to Zhong et al. (hereinafter "Zhong"). Claims 1-4, 6-7, 11-14, and 16-17 stand rejected under 35 U.S.C. 102(b) as being anticipated by "An Integrated Environment for HDL Verification", published in Verilog HDL Conference, 1995. Proceedings., by York et al. (hereinafter "York"). Claims 9-10 and 19-20 stand rejected under 35 U.S.C. 103(a) as being unpatentable over York in view of "The Verilog Procedural Interface for the Verilog Hardware Description Language", by

Dawson et al., and published in 1996 by IEEE (hereinafter "Dawson").